TECHNICAL WORK MAY NOT BEGIN PRIOR TO CTR ACCEPTANCE

NASA/GODDARD SPACE FLIGHT CENTER

REQUEST FOR TASK PLAN / TASK ORDER

CONTRACTOR	CONTRACT NO./TASK NO.	JOB ORDER NUMBER	APPROP. FY
QSS Group, Inc.	NAS5- 99124 TASK NO. 421 AMENDMENT	561-227-61-10-89	01

TASK TITLE: (NTE 80 characters; include Project name)

ICESat Spacecraft and GPS Receiver FPGA Design Overview

APPROVALS (Type or print name and sign)

	DATE	ORG CODE	MAIL CODE	PHONE
ASSISTANT TECHNICAL REPRESENTATIVE (OR TASK MONITOR) Robert W. Stone Robert W Stone	14 Nov 00	561	561	301-286-5659
BRANCH HEAD Robert W. Stone	DATE	CODE 561		PHONE 301-286-5659
CONTRACTING OFFICER'S TECHNICAL REPRESENTATIVE (COTR) Robert S. Lebair, Jr.	DATE 11/15/00	CODE 568		PHONE 301-286-6588

FLIGHT HARDWARE, CRITICAL GSE OR SOFTWARE? (IF YES, NEED CODE 303 CONCURRENCE NEXT BLOCK)	CONTRACTING OFFICER'S QUALITY REP.	DESIGNATED FAM:
[X] NO [ ] YES	Larry Moore	

The contractor shall identify and explain the reason for any deviations, exceptions, or conditional assumptions taken with respect to this Task Order or to any of the technical requirements of the Task Order Statement of Work and related specifications. The contractor shall complete and submit the required Reps and Certs.

(To be completed by Contracting Officer)
C.O. Requested Quote on:
Date:

Contractor will develop specification or statement of work under this task for a future procurement. [X] NO [ ] YES

Flight hardware will be shipped to GSFC for testing prior to final delivery. [ ] NO [ ] YES [X] N/A

Government Furnished Property/Facilities: [X] NO [ ] YES -- SEE LIST OF GFP (offsite only) / FACILITIES (onsite only)

Onsite Performance: [ ] NO [X] YES If yes: [ ] TOTAL [X] PARTIAL
If partial, indicate onsite work in SOW by asterisk (*)

Surveillance Plan Attached: [X] NO [ ] YES

Highlighted Contract Clauses: *(to be completed by Contracting Officer)*

The effective date of this Task Order shall be the date of the Contracting Officer's signature below.

INCENTIVE FEE STRUCTUR (check one)

	X No. 1	No. 2	No. 3	No. 4	No. 5
Cost	10%	50%	25%	25%	%
Schedule	15%	25%	25%	50%	%
Technical	75%	25%	50%	25%	%

(To be completed by Contracting Officer)

The target cost of this task order is $ 25,556.
The target fee of this task order is $ 1,637.
The total target cost and target fee of this task order as contemplated by the Incentive Fee clause of this contract is $ 27,193.

The maximum fee is $ 2,393.
The minimum fee is $0.

AUTHORIZED SIGNATURE

THIS TASK ASSIGNMENT IS ISSUED ACCORDING TO THE CONTRACT CLAUSE "TASK ASSIGNMENTS AND REPORTS"

Theresa J. Becker — SIGNATURE OF CONTRACTING OFFICER
12/8/00 — DATE
Theresa J. Becker — TYPED NAME OF CONTRACTING OFFICER

CONTRACTOR'S ACCEPTANCE

AUTHORIZED SIGNATURE — DATE

GSFC FORM 703-1845 12/98 (OLDER VERSIONS ARE OBSOLETE)

DISTRIBUTION: CONTRACTOR, CONTRACTING OFFICER, COTR, CODE 303, RESOURCES ANALYST, ASSISTANT TECHNICAL REPRESENTATIVE

TECHNICAL WORK MAY NOT BEGIN PRIOR TO CO APPROVAL

NASA/GODDARD SPACE FLIGHT CENTER

REQUEST FOR TASK PLAN / TASK ORDER

CONTRACTOR	CONTRACT NO./TASK NO.		
	NAS5-	TASK NO.	AMENDMENT
QSS Group, Inc.	99124	421	

Applicable paragraphs from contract Statement of Work: Function 2-5

STATEMENT OF WORK: (Continue on blank paper if additional space is required)

The contractor shall perform a design overview of the Field Programmable Gate Arrays (FPGAs) within the ICESat spacecraft (the Ball RS2000 bus) as well as within the ICESat Global Positioning System (GPS) receiver to determine whether the FPGA designs have followed the design guidelines contained within 561-PG-8700.2.1.

The Goddard ICESat Project, represented by Mike Tasevoli, 301-286-2321, shall provide hard copies or PDF files of the schematics, VHDL code, and any guidelines which were implemented during the FPGA development process to perform a brief evaluation (one each per FPGA) to identify areas of concern. This review will focus in on obvious design concerns and identify meta-stability issues which might impact operational performance.

This review and documentation of findings is estimated to take 12 hours per FPGA. Additional analysis may be necessary if the FPGA is in a critical application.

The evaluation shall be summarized in a report which includes an executive summary as well as a detailed summary of the design assessment.

Day-to-day technical direction shall be provided by Dennis Albaijes, Code 561, 301-286-0578, building 23, room E337.

PERFORMANCE SPECIFICATIONS:

Reports and Documents: Technical performance will be based on thoroughness and completeness of written reports. Acceptable performance is that the ATR is satisfied that the material reflects the proper level of technical expertise and meets the objectives of the activity. Reports shall be delivered to the ATR both as a hard copy and in PC compatible electronic format via email.

A **Final Report** shall summarize the effort. The report shall include a design assessment and recommendations for improvement, if necessary. Assessment of the overall design approach shall be validated against 561-PG-8700.2.1.

Technical Progress Report: Acceptable performance is that the ATR is satisfied that he is being kept informed of the status of work performed and of issues requiring his attention. Report to include: (1) summary of monthly progress; (2) plans for next month; (3) problems; (4) issues; and (5) resolution of problems/issues.

Management: Performance will be measured against the following metrics: (1) accomplishment of objectives; (2) clear, incremental progress; (3) responsiveness to issues; (4) efficient and appropriate staffing; and (5) coordination with and good working relationship with ATR and other related contractor efforts, if applicable.

APPLICABLE DOCUMENTS:

561-PG-8700.2.1

TASK END DATE: ~~1/15/01~~ 3/31/01

MILESTONES/DELIVERABLES AND DATES:

The timing of milestones/deliverables used to define schedule compliance does not begin until both:

a. The Project has furnished technical documentation as described in the Statement of Work, and
b. The CTR has been accepted.

1. FPGA Design Overview for first four FPGAs: due +10 business days
2. FPGA Design Overview for remaining eight FPGAs: due +20 business days
3. Final Report including executive summary and detailed backup: due +25 business days
4. Technical Progress Report: monthly, 15th of the month

PERFORMANCE STANDARDS:

Schedule: On-time deliver/completion of the deliverables/milestones
Technical: ATR's acceptance of the above

FINAL DELIVERY DESTINATION (NAME, BLDG, ROOM):

Robert W. Stone, building 23, room E305